IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s):	Azadet et al
Case:	14-6
Serial No.:	10/022,659
Filing Date:	December 18, 2001
Group:	2611
Examiner:	Juan A Torres
Title:	Method and Apparatus for Joint Equalization and Decoding of Multilevel Codes

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REPLY BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Appellants hereby reply to the Examiner's Answer, mailed September 19, 2007 (referred to hereinafter as "the Examiner's Answer"), in an Appeal of the final rejection of claims 1, 8, 16, 26 and 29 in the above-identified patent application.

REAL PARTY IN INTEREST

A statement identifying the real party in interest is contained in Appellants' Appeal Brief.

RELATED APPEALS AND INTERFERENCES

A statement identifying related appeals is contained in Appellants' Appeal Brief

STATUS OF CLAIMS

A statement identifying the status of the claims is contained in Appellants' Appeal Brief.

STATUS OF AMENDMENTS

A statement identifying the status of the amendments is contained in Appellants' Appeal Brief.

SUMMARY OF CLAIMED SUBJECT MATTER

A Summary of the Invention is contained in Appellants' Appeal Brief.

STATEMENT OF GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A statement identifying the grounds of rejection to be reviewed on appeal is contained in Appellants' Appeal Brief.

CLAIMS APPEALED

A copy of the appealed claims is contained in an Appendix of Appellants' Appeal Brief.

ARGUMENT

Independent Claim 16

Independent claim 16 was rejected under 35 U.S.C. §103(a) as being unpatentable over Raghavan in view of Trans. In the Grounds of Rejection portion of the Examiner's Answer, the Examiner again acknowledges that Raghavan does not disclose that a first binary value substantially always causes a *state transition in said trellis* from a first state to a different state and a second binary value does not cause a *state transition in said trellis*," as required by claim 16. See, Examiner's Answer, page 4, lines 8-10.

Later, in the Response to Arguments section of the Examiner's Answer, on page 15, second paragraph, the Examiner *contradicts* this admission, with an assertion that Raghavan discloses "for each particular state, that a first binary value substantially always maintains causes a state transition in the trellis from a first state to a different state and a second binary value does not cause a state transition in the trellis."

In any case, Raghavan explicitly discloses that a binary logic one (1) is transmitted as either a -1 or +1, and a binary logic zero (0) is transmitted as a 0 (see, col. 1, lines 24-36 and FIG. 1A) Again, Independent claim 16 requires that a first binary value, such as logic 1, causes a transition of the MLT-3 signal, and a second binary value, such as logic 0, leaves the MLT-3 signals unchanged. In Raghavan, however, (for example, Fig.1A), the input value 1 *sometimes* causes a transition into the same state, and sometimes causes a transition into a different state. Thus, one value does not *substantially always* lead to a state transition, as defined in claim 16

The Examiner also appears to allege that this limitation is not supported in the specification. Support for this limitation can be clearly found in the original specification, however, for example, at page 4, lines 17-18. Contrast, for example, the labels for the transitions in the trellis shown in FIG. 4 of the present application and FIG. 1A of Raghavan. The Examiner notes that the trellis *structure* is identical. As noted, however, what is significant is that the *labels* are different.

The Examiner asserts that Trans discloses that a first binary value substantially always causes a *state transition in said trellis* from a first state to a different state and a second binary value does not cause a *state transition in said trellis*," as required by claim 16. As previously asserted by Appellants, however, (but **again not** addressed by the Examiner in the Examiner's Answer), Trans teaches that each time a logic "1" is encoded, a transition (equal to an output value transition) will take place (there is no mention of causing a state transition in a trellis). Likewise, each time a logic 0 is encoded, the previous output level will be maintained for another bit period (again, there is no mention of causing a state transition in a trellis). See, Col. 61, lines 48-56. Trans does not disclose representing an MLT-3 code *using a trellis*, and thus, states or state transitions are not defined in Trans, as those terms are used by the present invention.

Raghavan thus teaches away from using Trans to achieve what is claimed by the present invention, as Raghavan does not define state transitions in the manner required by claim 16 *Compare,* the labels of the trellis of Raghavan to labels of the the MLT- trellis of the present invention. This "teaching away" is contrary to the combination suggested by the Examiner, even if both references are in the same field of endeavor (Ethernet communications). The Examiner furthers asserts that the motivation for the combination is a reduction of bandwidth and system complexity. It is noted that reduction of bandwidth and/or system complexity could be argued to motivate essentially all inventions in the communications field. This extremely general characterization cannot be said to support a combination of these specific references. Appellants assert that the only motivation for the asserted combination is the hindsight provided by the present invention.

Further, even if combinable, the references *collectively* do not teach each and every limitation of the independent claims. As indicated above, **Trans does not disclose representing an MLT-3 code using a trellis**, and thus, states or state transitions are not defined in Trans, as those terms are used by the present invention. Rather, Trans teaches that each time a logic "1" is encoded, a transition (equal to an output value transition) will take place (there is no mention of causing a state transition in a *trellis*). Likewise, each time a logic 0 is encoded, the previous output level will be maintained for another bit period (again, there is no mention of causing a state transition in a *trellis*). See, Col. 61, lines 48-56.

Thus, Raghaven and Trans, alone or in combination, do not disclose or suggest "generating each of said trellis states with at least two branches leaving or entering each state, each of said at least two branches corresponding to state transitions associated with said two binary values, wherein a first binary value *substantially always* causes a state transition in said trellis *from a first state to a different state* and a second binary value does not cause a state transition in said trellis," as required by claim 16.

Independent Claims 1 and 8

Independent claims 1 and 8 were rejected under 35 U.S.C. §103(a) as being unpatentable over Raghavan in view of Haratsch 1. In the Grounds of Rejection portion of the

Examiner's Answer, the Examiner again acknowledges that Raghavan does not disclose decoding a signal received from a dispersive channel causing intersymbol interference comprising generating at least one trellis representing the code and the dispersive channel; and performing joint equalization and decoding of the received signal using the trellis. See, Examiner's Answer, page 5, lines 15-18. The Examiner asserts, however, that this feature is shown by Haratsch 1

In the Response to Arguments section of the Examiner's Answer, on page 20, lines 13-16, the Examiner mischaracterizes the scope of claims 1 and 8, with a summary of what is captured by these claims. Appellants do not dispute that they may be broad claims, but assert that they are entitled to such broad claims based on the prior art.

The Examiner continues by noting that the secondary references used by the Examiner teach the use of joint equalization and decoding to reduce the complexity of the system, and that it "makes sense in the well-known MLT-3 system " Haratsch 1, however, is addressing trellis coded modulation (TCM) and not MLT-3 codes. Thus, it would not be obvious to a person of ordinary skill in the art to generate a trellis representing the MLT-3 and dispersive channel, in the manner suggested by the present invention

Furthermore, Haratsch 1 is addressing *four dimensional* TCM codes with 8 states. Thus, the corresponding computations disclosed by Haratsch 1, such as the branch metric computations, *do not make sense* in the context of the present invention. Thus, a person of ordinary skill in the art would not make this proposed combination. Furthermore, there is no enabling disclosure in Raghavan and/or Haratsch 1 of the appropriate branch metric computations for MLT-3 codes. For example, Equations 1 and 2 of Haratsch 1 do not make sense for MLT-3 codes, as they show the computation of the 1D ISI estimates and 1D branch metrics for each of the 4 dimensions. Page 466, left column, then shows how to combine the 1D branch metric to obtain 4D branch metrics for the 4D TCM code, which again does not make sense for MLT-3 codes. See also Figures 2 and 4, where one and four dimensional branch metric units are shown.

The Examiner supports the combination by asserting that both TCM and MLT-3 codes can be represented with a trellis structure, so it "makes perfect sense to interchange" them. As just indicated, however, it is not possible to merely interchange them The TCM-based

equations of Haratsch1 would not make sense in the context of Raghavan. Just because Haratsch1 addressed decoding of TCM codes does not suggest that it can be extended for decoding a MLT-3 encoded signal, as suggested by the present invention

In addition, as discussed hereinafter, if the combination was attempted in the manner suggested by the Examiner, an expression is obtained for the number of states that does not make sense The number of trellis states in Haratsch 1 is equal to the number of TCM code states and therefore equal to 8. In the present invention, on the other hand, the number of trellis states is $4x(2^K)$, where K is the truncated channel memory.

These incompatibilities between the combination of Raghavan/Haratsch 1 is contrary to the combination suggested by the Examiner, even if both cited references are in the same field of endeavor (Ethernet communications) Thus, a person of ordinary skill in the art would not make such a combination.

In addition to providing a different number of states, which suggests away from the combination, the minimum number of states associated with the present invention ($4x(2^K)=4$ for K=0) is lower than Haratsch 1. This is a "*surprising result*" which is further evidence of non-obviousness. This was **not** addressed by the Examiner in the Examiner's Answer.

Furthermore, the Examiner asserts that the motivation for combining Raghavan with Haratsch 1 would be to reduce the complexity of the system. Rather, claims 1 and 8 in fact generally increase the complexity of the system (joint equalization and decoding using a trellis representing both the MLT-3 code and dispersive channel) compared to a prior art system with a MLT-3 decoder and separate equalizer. This was **not** addressed by the Examiner in the Examiner's Answer.

Claims 26 and 29

With respect to claims 26 and 29, for example, the Examiner asserts that Haratsch 2 discloses that the number of states in the trellis is given by $4x(2^K)$, where *K is the truncated channel memory*. (citing page 171). In the passage of Haratsch 2 recited by the Examiner, however, the number of states is actually given by $Sx(2^{mL})$, where S is the number of TCM code states, m the number of bits that are fed into the TCM encoder, and *L is the **(full)** channel memory*.

m is defined in Fig 2 of Haratsch 2 for TCM codes, but is undefined for MLT-3 codes, which are different from TCM codes Significantly, the equation in page 171 of Haratsch 2 uses the channel memory L, while claims 26 and 29 use the truncated channel memory K Therefore, the equation in page 171 of Haratsch 2 is different and undefined for MLT-3 codes Thus, even if combinable (see arguments above), the references *collectively* do not teach each and every limitation of the independent claims In addition, there is no enabling disclosure for the application of Haratsch2 to MLT-3 codes (among other things, m is undefined for MLT-3 codes).

Dependent Claims

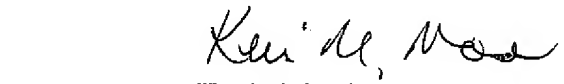
Claims 2, 7, 9-10, 12, 15 and 17-29 are dependent on claims 1, 8, or 16, and are therefore patentably distinguished over Raghavan, Haratsch 1, Trans, and Haratsch 2 (alone or in any combination) because of their dependency from independent claims 1, 8, and 16 for the reasons set forth above, as well as other elements these claims add in combination to their base claim

Conclusion

The rejections of the cited claims under section 103 in view of Raghavan, Haratsch 1, Trans, and Haratsch 2, alone or in any combination, are therefore believed to be improper and should be withdrawn. The remaining rejected dependent claims are believed allowable for at least the reasons identified above with respect to the independent claims.

The attention of the Examiner and the Appeal Board to this matter is appreciated

Respectfully,



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CLAIMS APPENDIX

1. A method for decoding a signal received from a dispersive channel causing intersymbol interference, said signal encoded using an MLT-3 code, said method comprising the steps of:

generating at least one trellis representing both said MLT-3 code and said dispersive channel; and

performing joint equalization and decoding of said received signal using said trellis.

2. The method of claim 1, wherein said performing step uses a reduced complexity sequence estimation technique

3 (Cancelled).

4 (Cancelled).

5 (Cancelled).

6. (Cancelled).

7. The method of claim 1, wherein said dispersive channel is an Ethernet channel.

8. A receiver for processing a signal received from a dispersive channel, said signal encoded using an MLT-3 code, comprising:

a sequence detector that performs joint equalization and decoding of said received signal using at least one trellis representing both said MLT-3 code and said dispersive channel.

9. The receiver of claim 8, wherein said sequence detector employs a reduced complexity sequence estimator.

10. The receiver of claim 9, wherein said reduced complexity sequence estimator employs a reduced-state trellis having a reduced number of states, wherein said reduced complexity sequence estimator further comprises:

a branch metric units (BMU) that calculates branch metrics based on said received signal;

an add-compare-select unit (ACSU) that determines the best surviving paths into said reduced states;

a survivor memory unit (SMU) that stores said best surviving paths; and

a decision-feedback unit (DFU) that takes survivor symbols from said SMU to calculate ISI estimates for said reduced states, wherein said ISI estimates are used by said BMU to calculate branch metrics for transitions in the reduced-state trellis.

11. (Cancelled)

12 The receiver of claim 8, wherein said sequence detector further comprises:

a branch metric units (BMU) that calculates branch metrics based on said received signal;

an add-compare-select unit (ACSU) that determines the best surviving paths into said trellis states; and

a survivor memory unit (SMU) that stores said best surviving paths

13. (Cancelled)

14. (Cancelled)

15. The receiver of claim 8, wherein said dispersive channel is an Ethernet channel

16. A method for representing an MLT-3 code as a trellis, said MLT-3 code using three signal levels to represent two binary values, said method comprising the steps of:

generating said trellis with a plurality of trellis states, each of said trellis states associated with a value for a signal in a previous symbol period; and

generating each of said trellis states with at least two branches leaving or entering each state, each of said at least two branches corresponding to state transitions associated with said two binary values, wherein a first binary value substantially always causes a state transition in said trellis from a first state to a different state and a second binary value does not cause a state transition in said trellis; and

using said trellis to decode a signal encoded using said MLT-3 code.

17. The method of claim 16, wherein a first one of said plurality of trellis states corresponds to a value for a signal in a previous symbol period of +1.

18 The method of claim 16, wherein a second and third of said plurality of trellis states corresponds to a value for a signal in a previous symbol period of 0.

19 The method of claim 16, wherein a fourth one of said plurality of trellis states corresponds to a value for a signal in a previous symbol period of -1

20 The method of claim 16, further comprising the step of using said trellis to perform joint equalization and decoding of a signal encoded using said MLT-3 code.

21 The method of claim 16, further comprising the step of combining said trellis with a trellis representing a channel to obtain a super trellis.

22. The method of claim 16, wherein said dispersive channel is an Ethernet channel.

23. The method of claim 1, wherein a state in said trellis is given by a concatenation of said MLT-3 code state and a channel state, wherein said channel state describes said dispersive channel.

24. The method of claim 1, wherein a state in said trellis is given by a concatenation of said MLT-3 code state and a truncated channel state, wherein said truncated channel state partially describes said dispersive channel.

25. The method of claim 24, further comprising the steps of computing ISI estimates for said states using symbols from corresponding survivor paths; computing branch metrics for transitions in said trellis based on said ISI estimates; determining survivor paths into said states based on said branch metrics; and storing said survivor paths

26. The method of claim 24, wherein a number of states in said trellis is given by $4x(2^K)$, where K is the truncated channel memory.

27. The receiver of claim 8, wherein a state in said trellis is given by a concatenation of said MLT-3 code state and a channel state, wherein said channel state describes said dispersive channel.

28. The receiver of claim 8, wherein a state in said trellis is given by a concatenation of said MLT-3 code state and a truncated channel state, wherein said truncated channel state partially describes said dispersive channel

29. The receiver of claim 28, wherein a number of states in said trellis is given by $4x(2^K)$, where K is the truncated channel memory.

EVIDENCE APPENDIX

There is no evidence submitted pursuant to § 1.130, 1.131, or 1.132 or entered by the Examiner and relied upon by appellant.

RELATED PROCEEDINGS APPENDIX

There are no known decisions rendered by a court or the Board in any proceeding identified pursuant to paragraph (c)(1)(ii) of 37 CFR 41.37.